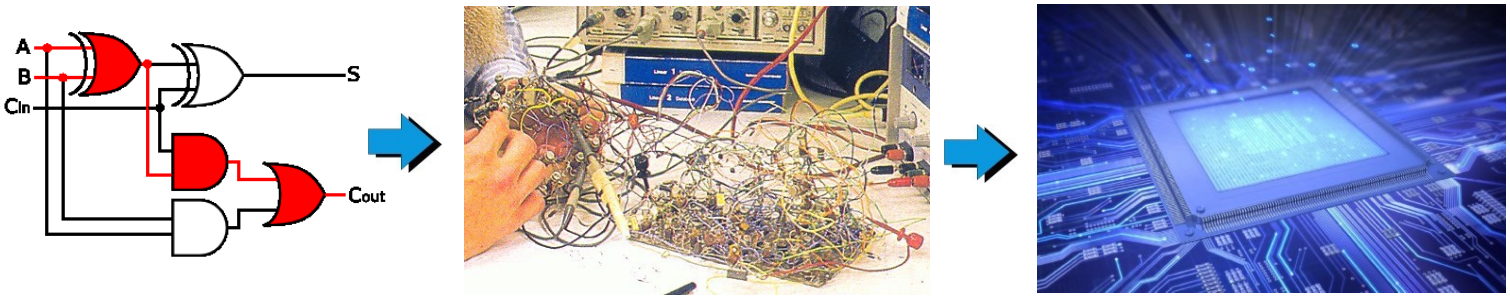
# Summer 2017 – Online Course Offering

## EELE 261 – Introduction to Logic Circuits (4cr)

### Montana State University - Bozeman

Instructor: Dr. Brock J. LaMeres



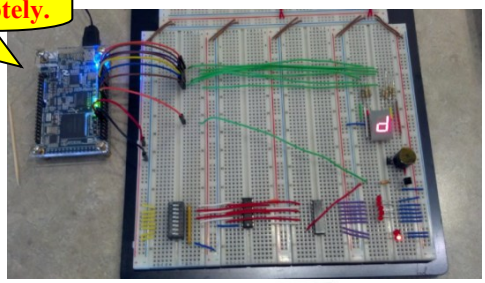

**Are you a EE/CpE student that wants to gain 4-credits toward your degree while you're off-campus this summer? Are you a CS student that wants to work toward a EE/CpE minor? Then this fully online course is for you!**

**Course Description**

This course introduces the concepts of classical digital logic design including number systems, interfacing, Boolean algebra, combinational logic design, and finite state machines. This course also covers Hardware Description Languages for the structural design and simulation of digital systems. Modern digital design of combinational logic and state machines is covered using VHDL and a logic synthesizer. This course contains a laboratory experience where students design and implement logic circuits using discreet parts and programmable logic devices.

**Course Logistics**

**A lab kit will be provided to accomplish all experiments remotely.**



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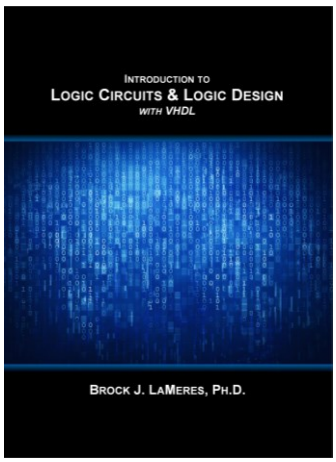
| Prerequisites: | College algebra. |
| Dates: | 12-week summer session, May 16th to August 8th. |
| Lecture (3cr): | The course will follow the textbook exactly. There will be short lecture videos provided for each section. Homework and exams will be in the form of online multiple choice quizzes or logic simulations that will be uploaded to the course DropBox. |
| Lab (1cr): | A portable lab kit will be checked out that will allow all of the lab experiments to be performed remotely. Lab demonstrations will be conducted using Google+ Hangout video conferencing or by uploading videos of your demonstrations. Students will use electronic lab notebooks. |
| Requirements: | The textbook (available from the MSU bookstore or in eBook form) and a computer with video conferencing capability and that is fast enough to run the Altera Quartus II / ModelSim software tools. |

**The *Analog Discovery* USB oscilloscope will be used to take measurements.**


**Flexibility**

This course is designed to be accomplished completely online, including the laboratory component. The class is laid out to follow the 12-week summer session with weekly deadlines. However, if you would rather follow the 6-week session, suggested deadlines will be provided that will follow either the 1st session or 2nd summer session.

**Textbook**

Introduction to Logic Circuits & Logic Design with VHDL
by Brock J. LaMeres (note: this book was designed specifically for this course).

## Course Outline

### MODULE 1: INTRODUCTION – ANALOG VS. DIGITAL

1.1 Differences between Analog and Digital Systems
1.2 Advantages of Digital Systems

### MODULE 2: NUMBER SYSTEMS

2.1 Positional Number Systems
2.2 Base Conversion
2.3 Binary Arithmetic
2.4 Unsigned and Signed Numbers

### MODULE 3: DIGITAL CIRCUITRY & INTERFACING

3.1 Basic Gates
3.2 Digital Circuit Operation
3.3 Logic Families
3.4 Driving Loads

### MODULE 4: COMBINATIONAL LOGIC DESIGN

4.1 Boolean Algebra
4.2 Combinational Logic Analysis
4.3 Combinational Logic Synthesis
4.4 Logic Minimization
4.5 Timing Hazards & Glitches

### MODULE 5: VHDL (PART 1)

5.1 History of Hardware Description Languages
5.2 HDL Abstraction
5.3 The Digital Design Flow
5.4 VHDL Constructs
5.5 Modeling Concurrent Functionality in VHDL
5.6 Structural Design Using Components
5.7 Overview of Simulation Test Benches

### MODULE 6: MSI LOGIC

6.1 Decoders (classical design + VHDL)
6.2 Encoders (classical design + VHDL)
6.3 Multiplexers (classical design + VHDL)
6.4 Demultiplexers (classical design + VHDL)

### MODULE 7: SEQUENTIAL LOGIC DESIGN

7.1 Sequential Logic Storage Devices
7.2 Sequential Logic Timing Considerations
7.3 Common Circuits Based on Sequential Storage Devices
7.4 Finite State Machines
7.5 Counters
7.6 Finite State Machine’s Reset Condition
7.7 Sequential Logic Analysis

## Grading

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| Homework | 25% |
| Lab Experiments | 25% |
| Module Quizzes | 25% |
| Midterm Exam | 10% |
| Comprehensive Final Exam | 15% |