Department	Electrical and Computer Engineering
Course Number	**EE 414**
Course Title	Introduction To VLSI Design
Course Designation	Elective
University Catalog Description	Semesters offered: F; Prerequisites: EE262, EE317 -- Introduction to the fundamentals of CMOS VLSI circuit design. This course covers CMOS device characteristics and timing, CMOS fabrication, CAD tools, design rules, simulation and layout, CMOS combinational and sequential logic, SRAM and DRAM memory, and dynamic logic design.
Faculty Coordinator	Dr. Brock J. LaMeres
Prerequisite by Topic	Linear Electronics, MOSFET transistors, combinational and sequential logic circuits.
Textbook	"CMOS Digital Integrated Circuits" 3rd Edition, Sung-Mo Kang and Yusuf Leblebici, McGraw Hill, 2003
Course Objectives	This course is intended to give students an introduction to the design and layout of custom digital integrated circuits. Students are expected to learn how integrated circuits are fabricated, understand the operation of MOSFET transistors, use CAD tools to create mask definitions for fabrication. Students will understand logic gates, memory elements and testability.
Course Learning Outcomes	At the conclusion of EE 414, students are expected to : 1) Create an integrated circuit layout from a schematic. 2) Create a schematic from an integrated circuit layout. 3) Perform transistor level design and layout of a custom state machine. 4) Verify performance of CMOS circuits using hand calculations and circuit simulators such as Spice. 5) Describe the photo-resist based etching process. 6) Describe the self-aligned CMOS transistor fabrication sequence. 7) Design a complex CMOS logic gate from a truth table.
Topics Covered	1) Fabrication of CMOS integrated circuits. 2) Basic physical operation of a MOS transistor including depletion regions, inversion layers, channel inch-off, reverse bias diode capacitance and gate capacitance. 3) Calculation of drain current using oxide capacitance, threshold voltage, mobility, body effect and channel length modulation. 4) Spice Level 1 and Bsim3 model parameters. 5) Use of MOS transistors in logic gates flip flops and memory. 6) Complex logic gates. 7) Flip-flops and latches. 8) State Machine design using CMOS Logic Gates. 9) Integrated Circuit Layout techniques, CAD tools and computer layout checking. 10) Parasitic SCR Latch-up and substrate contacts. 11) Packaging 12) Design for test.
Class/Laboratory Schedule	EE 414 meets two times /week for 75 minutes
Professional Component (Criterion 5)	Students use an industrial strength Spice and IC Layout CAD tool for homework problems and a project.
ECE Program Outcomes	EE 414 supports following Program Outcomes: n/a
Total Credit Hours	3
Prepared by	Brock J. LaMeres 5/19/2009